WAYTRONX™

The coolest path to system performance.™

White Paper

Waytronx 3C for 3D Packaging Roadmap

What is 3D Packaging?

3D packaging, where integrated circuits (ICs) are combined, stacked and interconnected, can combine CPUs, memory, logic, sensors and optoelectronics into a much smaller, thinner and more powerful form factor than traditional horizontal 2D packaging. The industry megatrend is moving from current 2D packaging to 3D stacking, with wires or surface bump bonding with vias for connections. More advanced 3D ICs may utilize Through-Silicon Via (TSV) interconnects to reduce footprint, increase silicon efficiency and create shorter communication interconnects.

The growing importance of 3D packaging has prompted the SEMATECH semiconductor consortium and other industry organizations to develop roadmaps for 3D IC packaging requirements. Commercialization is beginning for 3D packaging, with a shift away from 2D packaging occurring over the next five to 10 years. 3D packaging is a design decision that must be made before circuit design is started.

Now, Waytronx, Inc., the leading openly licensable thermal management solutions company, has developed a 3D solution, called the **Waytronx *3C for 3D* Packaging Roadmap.** Only Waytronx has developed a comprehensive approach to 3D packaging that incorporates **cooling, communications and current (power) into a single system**. Unlike other options, all the performance attributes are designed in, rather than added on after the silicon design limits have been reached.

3D Packaging Advantages

"3D integration will establish a new scaling path that will extend Moore's Law beyond its expected limits," noted Steven Koester, manager of exploratory CMOS technology at IBM (East Fishkill, N.Y.), in a recent webcast, "Ultra Thin Wafer Processing Solutions."[1]

3D packaging can provide several benefits:

- **Overcome 2D wiring limitations**

  Today's practical bus widths are a couple of hundred pins. Today, higher speed peripheral component interconnect (PCI) and other common busses require retiming and regeneration to deal with long

horizontal lengths. Large amounts of power and space are wasted, and a cooling problem is created.

- **Increase system performance**

  High speed interconnections are necessary to keep system performance close to on-chip performance. 3D packaging can shorten communications paths, increase bus speeds, and open up performance through more economic parallel, fabric communications.

- **Reduce power consumption**

  A significant percentage of system power consumption occurs in boosting signals and combating low signal to noise in high speed chip interconnections.

- **Integrate diverse technologies**

  Integrating analog, mixed signal and digital functions on a chip may be difficult or uneconomic at the die level. Multiple operating voltages and different di/dt responses can make single chip design difficult. In digital chips, embedded memory may be expensive when fabricated in leading edge technologies. By separating these functions and recombining them in 3D packaging, costs are reduced and performance is increased.

- **Faster time to market**

  By stacking chips together, known good functions from previous-generation IP can be quickly integrated to achieve faster time to market. Development and engineering costs are reduced. System functionality can be proven prior to production.

Applications for 3D Packaging

The market for 3D integration includes many applications ranging from imaging products and memory to high-speed logic and processing applications. Some 3D integration is planned for military-related products. Applications are expected to include wire-limited circuits, such as gate arrays, systolic arrays, memory and imaging. The main driver is denser circuitry that results in improved electrical performance.

Microprocessors: Avoiding performance loss due to interconnect delays may be achieved through direct stacking of processors, chipsets, memory and graphics. In an interview with CNET News.com at the Fall 2006 Intel Developer Forum, Intel's Chief Technology Officer Justin Rattner described a processor with 80 cores on a single piece of silicon with up to a terabyte/second of computing power.[2] The main performance problems with an 80-core processor are off chip, providing enough I/O communications capacity and memory latency. 3D packaging is a likely solution to this need for massively parallel bandwidth and low latency.

Since processors generate more heat than the memory, 3D packages with the proper thermal management solutions are needed. Rattner concluded that "We will do a lot of work with it [packaging] in the next several years."[3]

Memory: In memory stacks, 3D integration can provide a 1000X increase in speed and a 100X decrease in power consumption. The transfer rate between chips is in the terabyte/second range, and there is the potential for a massively parallel I/O architecture. In April 2007, Samsung Electronics announced that it has developed the first all-DRAM stacked memory package using TSV technology. Its new wafer-level-processed stacked package (WSP) will not only reduce the overall package size but also permit chips to operate faster and use less power. Samsung noted that its advanced WSP technology, which can be utilized in diverse combinations of semiconductor packaging including system-in-package solutions, supports the rapid industry demand for high density, high performance semiconductor solutions for next-generation computing.

System on a Chip (SOC): 3D packaging enables performance gains and design flexibility in a tiny form factor. 3D packaging enables diverse analog, mixed signal, power and digital processing chips to achieve the performance of integrated design at much lower cost and complexity.

Limits to 3D packaging

Problems presented by 3D packaging include microwarming, power and signal routing, low yield and limited rework.

Microwarming is a major limiter to 3D packaging. Microwarming starts at the tiniest element of digital electronics, the transistor, and extends to the integrated environment within and surrounding advanced devices. In fact, microwarming is pervasive in every level of digital integration. Today's CPUs,

memory chips, SOCs, graphics processors and all ICs are generating ever larger amounts of performance-limiting heat.

Figure 1 shows the power density progression of CMOS processors and the resulting clock speed limitations. Dense 3D packaging of such processors exacerbates the problem by concentrating more heat in a confined area. 3D packaging solutions will require integrated cooling technology to address microwarming.

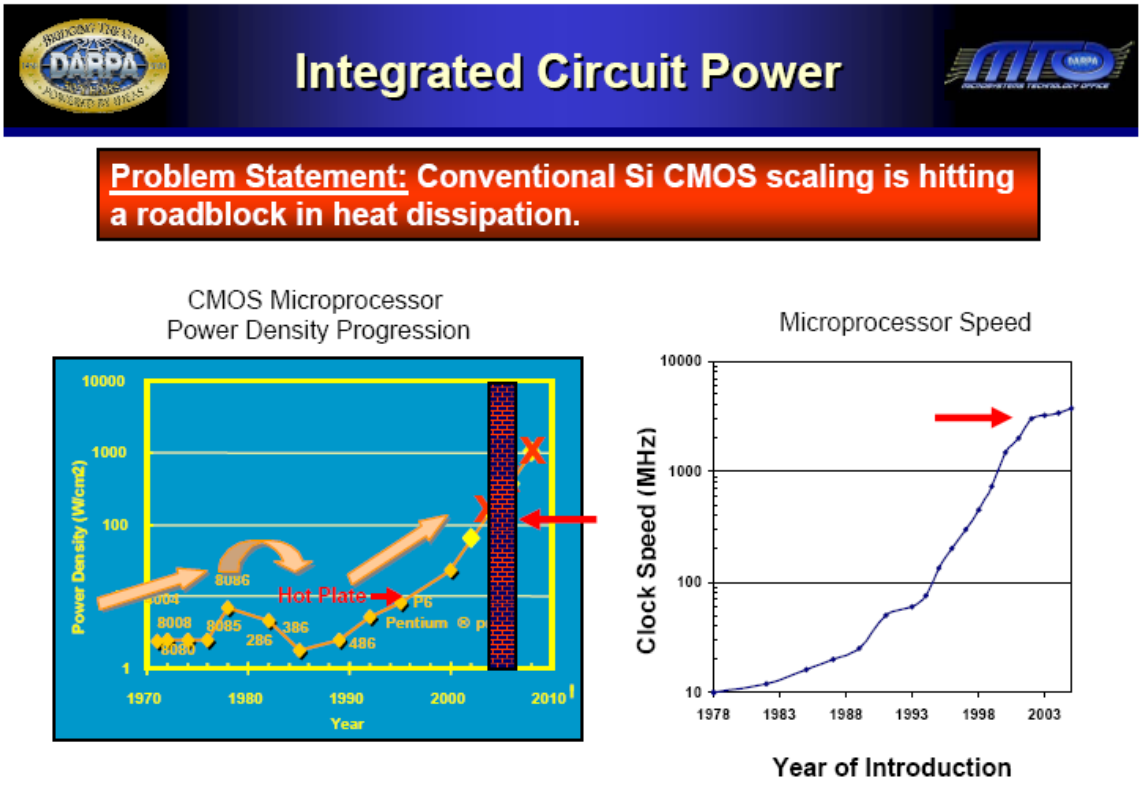

Figure 1: DARPA Microsystems Technology Office, March 2007

Waytronx 3C for 3D Roadmap

Waytronx *3C for 3D* technology roadmap addresses 3D packaging issues in a very cost effective manner. 3C indicates ***Cooling, Communications and Current*** delivery in an integrated packaging system as seen in Figure 2.

The Waytronx *3C for 3D* technology roadmap solves microwarming, power and signal routing, manufacturing yield and system rework in a single comprehensive architecture.

The Waytronx *3C for 3D* technology roadmap allows semiconductor die to have integrated circuits on both sides of the die by providing more effective means of power, communication and heat transport.

The Waytronx *3C for 3D* technology roadmap provides a low risk upgrade path for today's systems. As today's systems transition from 2D packaging to 3D packaging solutions, the same WayCool™ architecture being utilized in today's high performance systems provides the starting point for 3D packaging, based on the WayCool™ Hybrid Mesh interposer.

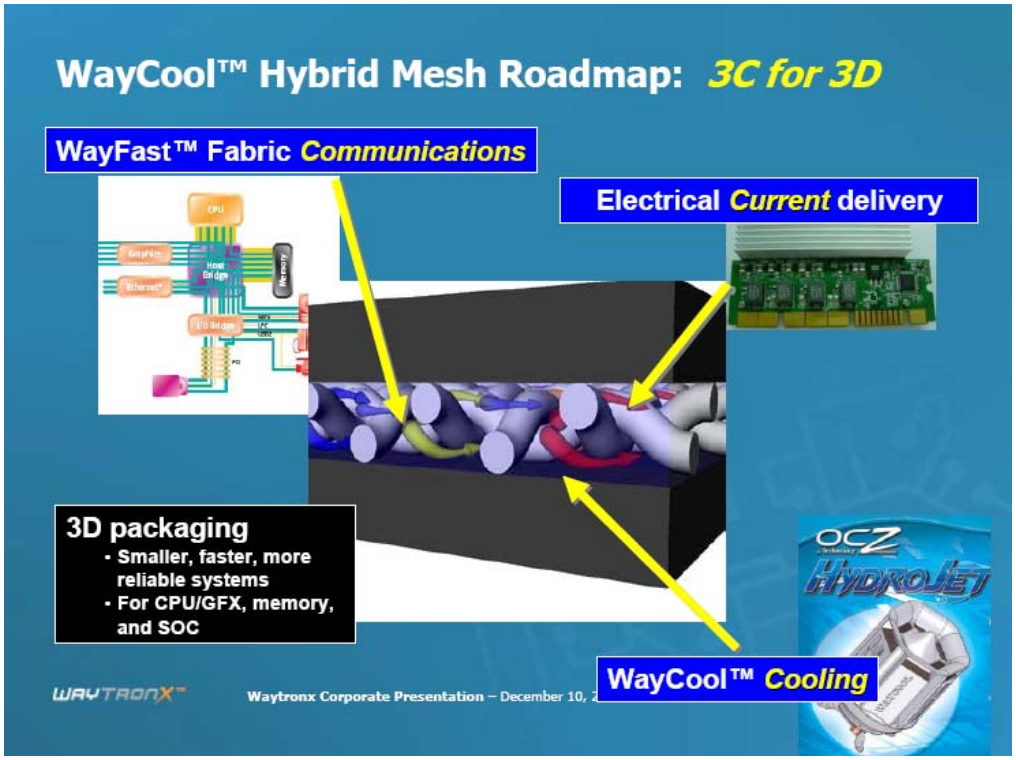

Figure 2: Waytronx *3C for 3D* Technology based on WayCool Hybrid Mesh

Way Cool™ Hybrid Mesh: WayCool Hybrid Mesh is a patented structural integrity component of the architecture and liquid carrier that provides complete flexibility of form factor for cooling. WayCool Hybrid Mesh is the key component in the WayTronX ***3C for 3D*** **Packaging Technology Roadmap.** WayCool Mesh design acts as a fully compliant interposer and enables the addition of *communications* (I/O) and *current* (power) to WayCool Architecture's industry-leading *cooling* capabilities in a single integrated packaging solution.

WayCool Hybrid Mesh provides the means to access a large number of locations on one or both faces of each die. Electrical and photonic communication can easily be coupled to off die input/output circuitry by extending the mesh beyond the die edges. WayCool Hybrid Meshes may be used in conjunction with or as an addendum to conventional integrated circuit routing schemes. Figure 3 shows an example of multiple die in a multiple Hybrid Mesh stack incorporating both electrical and optical i/o.

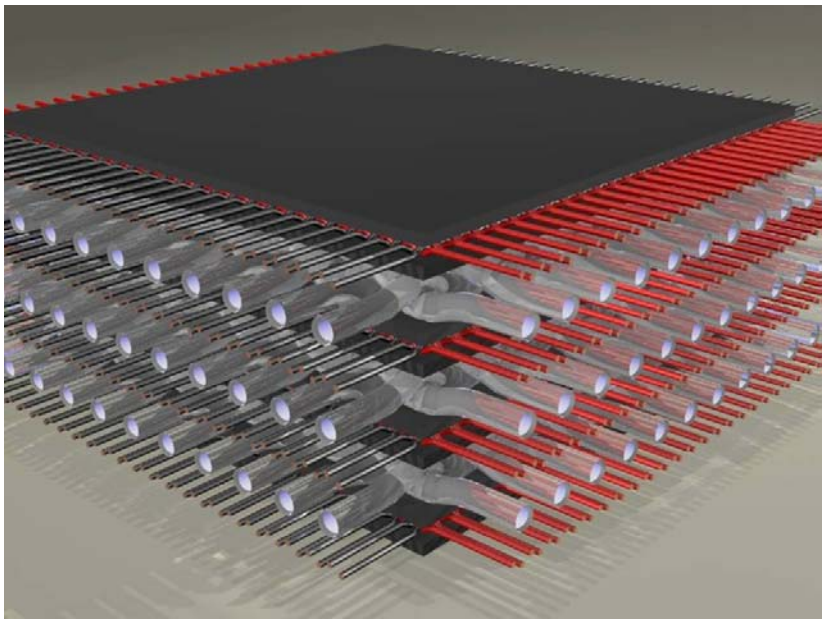

Figure 3: Multiple die stack with alternating optical conduit arrays and electrical conduit

WayCool Hybrid Meshes are the most flexible of any 3D design substrates. WayCool Hybrid Meshes can be configured with fine conductive metal wires and/or photonic conductors in one or both axis, as required by the

application. WayCool Hybrid Meshes may be bump soldered to one die face and pressure contacted to the opposing die face. This bonding scheme may aid alignment during assembly. Mesh materials may be chosen to match or mediate the die coefficient of thermal expansion (CTE).

3D electronic systems have also been costly to manufacture because of the difficulties associated with the large number of communication and power transport links required and the limited ability for rework. WayCool™ Hybrid Mesh uses compliant pressure type contacts, and thereby allows easy rework, removing the need for soldering or die bonding and the issues resulting from elevated process temperatures.

WayCool™ Architecture for *Cooling* is a hybrid (air + liquid) thermal management architecture consisting of passive and active elements designed to work both independently to effectively cool systems and to be combined in unique solutions called reference designs. Key elements of WayCool architecture (see Figure 1) include:

- WayCool™ Carbon Block technology for up to 4X conductive heat transfer
- WayCool™ Mesh
- WayCoolant™ Coolant is the ideal fluid designed for WayCool Mesh
- WayCool Hermetically Sealed Pumps
- WayCool Heat Sinks
- WayCool Quiet Fans

The WayCool Hybrid Mesh provides a thermal management plane. The highly parallel fluid manifold is designed into the 3D packaging system, rather than added on later. Highly dense 3D packaging structures, where watts per square meter may be much higher than traditional 2D packaging, require these "thermal ground planes." WayCool architecture components provide the complete solution to removing heat from dense 3D packaging.

WayFast™ *Communications* Technology

The Waytronx 3D packaging technology includes layers of WayCool™ woven meshes in direct contact with semiconductor chip surfaces. The meshes may be made with electrical power delivery and/or wire line communications in one or two axis and an optional short distance parallel optical fiber communications in the opposite axis. This allows high speed power management and data communications at enormously increased rates.

WayFast™ Electrical I/O: 3D packaging schemes typically require offsets for wire bonding and multilayered circuit boards at the top and/or bottom of the stack to provide I/O connectivity. WayCool™ Hybrid Mesh interposers provide I/O opportunities at each layer.

The electrical addressability of the mesh may be increased by including the use of diodes or transistors at the X-Y mesh crossings. The diodes or transistors may be part of the dies integrated circuitry and can provide for individually addressing any X-Y point on the die. Additional electrical addressability means include the use of multi-conductor conduits e.g. coaxial, triaxial, twisted pair, twisted group or helically plated conduits.

Woven wire meshes may also aid in EMI/RFI shielding and grounding.

WayFast communication systems may be particularly attractive for massively parallel, neural net, and switched fabric I/O specifications.

WayFast™ Optical I/O: As silicon lasers, VCSELs and parallel optical buses continue to improve and evolve, WayFast Communications provides a convenient integration path for optical communications. WayCool Hybrid Mesh provides a convenient upgrade path to transition from electrical to optical I/O or even combine the two types of I/O in 3D packaging.

Moving beyond today's optical to electrical to optical termination data conversions, Free Space Optical Communication may reduce the need for the close tolerances typically required in the manufacture and integration of parallel optical components.

Optoelectronics promises greatly increased operating frequencies and bandwidth but comes with the need to transport heat from the emitters. Combining WayFast I/O with WayCool architecture can provide the heat transport rates needed to make optoelectronic systems more attractive. Optical clocking may greatly reduce timing fan-out problems. Figure 4 shows an example optical i/o arrangement between two die.

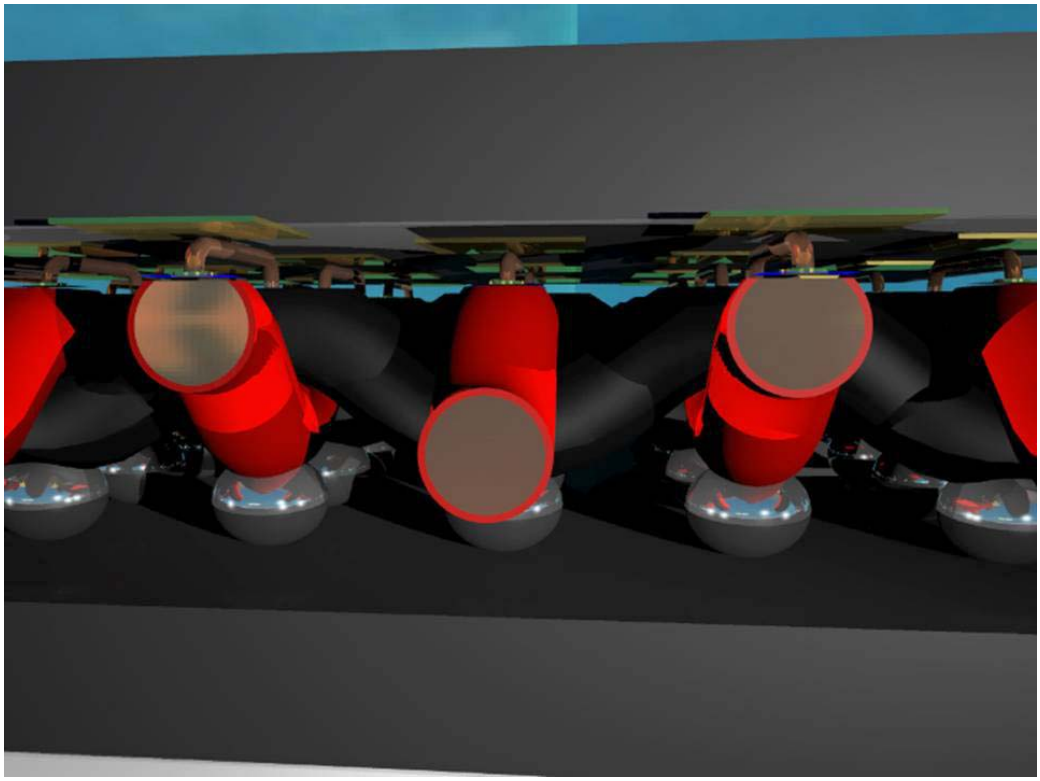

Figure 4: Section view of WayCool Hybrid Mesh array with LED array communicating with detector array on neighboring die face

Waytronx Electrical *Current* Power Delivery System

WayCool™ Hybrid Mesh may be configured to create very high power density inductors and resistors and thereby allow these components to be reduced in cost and number, placed in much closer proximity, and operated at greatly increased power density and frequency. Switchable resistor arrays with very high power density can provide power supplies with a wide range of voltage or current in a very small space and at very low cost.

Die regions may be electrically isolated and transfer power to other regions of the die or to other components solely via the WayCool Hybrid Mesh.

Waytronx *3C for 3D* roadmap

For more information, visit www.waytronx.com

[1] Steven Koester, "Ultra Thin Wafer Processing Solutions," *Semiconductor International Webcast*, June 20, 2007

[2] Michael Kanellos, "Processor, Memory May Marry in Future Computer," *CNET News.com*, September 28, 2006

[3] Samsung Electronics Co., Ltd., press release, "*Samsung Electronics Develops New, Highly Efficient Stacking Process for DRAM*," April 22, 2007